

LISTING OF THE CLAIMS:

1. (Currently amended) A crack stop for an integrated circuit (IC) chip having an active circuit area, comprising:

the IC chip including a bottom substrate, metal layers separated by capping layers, a top aluminum layer, and copper or silver metal interconnects which do not form a self-passivating oxide layer, in a low-K dielectric material;

a moisture barrier/edge seal positioned along the outer peripheral edges of the active area of the IC chip;

a crack stop formed by at least one trench or void region outside of the moisture barrier/edge seal on the outer periphery of the IC chip and extending substantially completely between the bottom substrate and the top aluminum layer of the IC chip, for preventing damage to the active area of the IC chip caused by chipping and cracking formed along peripheral edges of the IC chip during a dicing operation performed on the IC chip.

Claims 2 and 3 (Cancelled).

4. (Original) The crack stop for an IC chip as in claim 1, wherein the moisture barrier/edge seal comprises at least one inner boundary moisture barrier/edge seal formed by a metal stack around the active circuit area of the IC chip.

5. (Original) The crack stop for an IC chip as in claim 4, wherein each metal stack comprises a number of metal lines and via bars.

6. (Original) The crack stop for an IC chip as in claim 1, wherein the crack stop comprises a plurality of trenches or void regions formed outside of the moisture barrier/edge seal on the outer periphery of the IC chip.

7. (Currently Amended) A crack stop structure for preventing damage to an active area of an integrated circuit (IC) chip due to edge chipping and cracking from a dicing operation, comprising:

the active area of the IC chip comprising a bottom substrate, metal layers separated by capping layers, a top aluminum layer, and copper or silver interconnects which do not form a self-passivating oxide layer in a low K dielectric material;

a crack stop and a moisture barrier/edge seal, wherein the crack stop comprises a trench or groove on the outer periphery of the IC chip and extending substantially completely between the bottom substrate and the top aluminum layer of the IC chip, and the moisture/barrier edge seal comprises a metal stack between the crack stop and the active area of the chip.

8. (Withdrawn) A method for forming a crack stop for an integrated circuit (IC) chip having an active circuit area, wherein the IC chip includes metal interconnects which do not form a self-passivating oxide layer, in a low-K dielectric material, and a moisture barrier/edge seal positioned along the outer peripheral edges of the active area of the IC chip, at least one outer boundary crack stop formed by at least one trench or groove outside of the moisture barrier/edge seal on the outer periphery of the IC chip for preventing damage to the active area of the IC chip caused by chipping and cracking formed along peripheral edges of the IC chip

during a dicing operation performed on the wafer, the method comprising:

forming the IC chip on the wafer substantially to completion but without a final top aluminum Al layer;

forming the crack stop and the moisture barrier/edge seal by making a series of stacked via structures that form a boundary around the outer peripheral edges of the active area of the IC chip;

forming a top Al layer over the IC chip, without forming the Al layer on the regions of the crack stop, while forming the Al layer on the regions of the moisture barrier/edge seal, inside the perimeter of the crack stop, to protect the edge seal regions from a subsequent wet etch;

etching the wafer in a wet etch that removes the metal interconnect and barrier layers selective to Al, to form an etched out region as a crack stop.

9. (Withdrawn) The method of claim 8, including etching the wafer in a wet etch comprising dilute H₂SO₄:H₂O₂:HF.

10. (Withdrawn) The method of claim 8, including etching the wafer in a wet etch comprising dilute H₂SO₄:H₂O₂.

11. (Withdrawn) The method of claim 8, including forming the metal interconnects as copper interconnects.

12. (Withdrawn) The method of claim 8, including forming the metal interconnects as silver interconnects.

13. (Withdrawn) The method of claim 8, including forming the moisture barrier/edge seal by forming at least one inner boundary moisture barrier/edge seal by a metal stack around the active circuit area of the IC chip.

14. (Withdrawn) The method of claim 8, including forming each metal stack by forming a number of metal lines and via bars.

15. (Withdrawn) The method of claim 8, including forming at least one outer boundary crack stop as an etched out void region formed around the outer peripheral edges of the at least one inner boundary moisture barrier/edge seal.